IN THE CLAIMS:

1. (Currently Amended) An adaptive equalization circuit, comprising:

an analog-digital conversion device for sampling signals read from a recording medium;

a first digital equalization device for equalizing ~~the~~ waveforms of first output signals ~~of~~ from said analog-digital conversion device;

a phase synchronization device for synchronizing phases for second output signals ~~equalized by~~ from said first digital equalization device;

an equalization target value generation device for generating an equalization target value of said first digital equalization device from ~~the signals having phases being synchronized by~~ third output signals from said phase synchronization device, and for outputting fourth output signals; and

a first factor computation device for receiving as input signals said first, second, and fourth output signals, and for computing tap factors of said first digital equalization device from ~~the output of said analog-digital conversion device, the signals equalized by said first digital equalization device, and said equalization target value~~ said first, second, and fourth output signals.

2. (Currently Amended) The adaptive equalization circuit according to Claim 1, wherein said equalization target value generation device further comprises[:]

a temporary target value generation device for generating a temporary target ~~value~~ value, that is the equalization target value of the phase-synchronized signals, and

an equalization target phase rotation device for generating a true target ~~value that is~~ value, from said temporary target value, the true target value being an equalization target value before synchronizing phases by said phase synchronization device~~, from said temporary target value~~.

3. (Previously Presented) The adaptive equalization circuit according to Claim 1, wherein said first digital equalization device is an FIR filter having tap factors of a symmetric type.

4. (Currently Amended) The adaptive equalization circuit according to Claim 1, further comprising a second digital equalization device for inputting the third output signals ~~having phases being synchronized by~~ from said phase synchronization device and performing adaptive equalization, and a second factor computation device for computing the tap factors of said second digital equalization device from the third output signals ~~having phases being synchronized by~~ from said phase synchronization device and ~~the~~ fifth output signals ~~equalized by~~ from said second digital equalization device.

5. (Original) The adaptive equalization circuit according to Claim 4, wherein said second digital equalization device is a FIR filter having tap factors of an asymmetric type.

6. (Currently Amended) The adaptive equalization circuit according to Claim 2, wherein said phase synchronization device is a phase synchronization loop comprising a first interpolation device for interpolating the second output signals ~~equalized by~~ from said first digital equalization device and an interpolation position computation device for computing an interpolation position of said first interpolation device from ~~the~~ sixth output ~~of~~ signals from said first interpolation device, and

said equalization target phase rotation device ~~being~~ is a second interpolation device for interpolating said temporary target value and acquiring said true target value, ~~the~~ an interpolation position of said second interpolation device being computed by said interpolation position computation device.

7. (Currently Amended) The adaptive equalization circuit according to Claim 6, wherein said first interpolation device and second interpolation device are FIR filters, said interpolation position computation device ~~outputting~~ outputs tap factors as information of the interpolation position, and if each tap factor is COE(n) where n is the number of taps, the tap factor h1 to be supplied to said first interpolation device is given by h1 = {COE(1) COE(2) COE(3) - - - COE(n)}, and wherein

when the number of taps of said second interpolation device is the same as the number of taps of said first interpolation device, the tap factor h2 to be supplied to the second interpolation device has a symmetrical relationship with said h1, that is given by h2 = {COE(n) COE(n-1) COE(n-2) - - - COE(1)}, or the factor h2 is delayed and input to the second interpolation device,

when the number of taps of said second interpolation device is different from the number of taps of said first interpolation device, h3, that is a factor having a phase characteristic equivalent to said h1, is given by h3 = {COE(1) COE(2) COE(3) - - - COE(m)}, where m is a number of taps, and

the tap factor h4 to be supplied to said second interpolation device has a symmetrical relationship with said h3 and is given by h4 = {COE(m) COE(m-1) COE(m-2) - - - COE(1)}, or the factor h4 is delayed and input to said second interpolation device.

8. (Currently Amended) The adaptive equalization circuit according to Claim 3, wherein ~~even if phase synchronization performed by said phase synchronization device is in an unlock status,~~ said first factor computation device supplies the computed tap factors to the first digital equalization device and performs adaptive equalization regardless of whether phase synchronization performed by said phase synchronization device is in an unlock status.

9. (Currently Amended) The adaptive equalization circuit according to Claim 3, further comprising a frequency error monitor for monitoring ~~the~~ frequency errors of the phase synchronization performed by said phase synchronization device, wherein when said frequency error is smaller than a predetermined value, said first factor computation device supplies ~~the~~ computed tap factors to the first digital equalization device and starts adaptive equalization.

10. (Original) The adaptive equalization circuit according to Claim 9, further comprising a frequency locking device for changing the frequency information to be used for computation by said interpolation position computation device so as to decrease the frequency errors detected by said frequency error monitor.

11. (Currently Amended) An adaptive equalization method for equalizing signals read from a recording medium to a desired characteristic, comprising:

reading first signals from a recording medium;

sampling ~~the read~~ said first signals and outputting sampled second signals;

equalizing waveforms for the sampled second signals and outputting waveform-equalized third signals;

performing phase synchronization for the waveform-equalized third signals and outputting phase-synchronized fourth signals;

generating ~~an equalization target value of said waveform equalization~~ a fifth signal from the phase-synchronized fourth signals, said fifth signal corresponding to an equalization target value of said waveform equalization; ~~and~~

receiving said second, fourth, and fifth signals as inputs to a first factor computation device; and

computing tap factors with said first factor computation device for said waveform equalization from said ~~sampled signals, said waveform-equalized signals, and said equalization target value~~ second, fourth, and fifth signals.

12. (Currently Amended) An adaptive equalization method for equalizing signals read from a recording medium to a desired characteristic, comprising:

reading first signals from a recording medium;

sampling the read first signals and generating sampled second signals;

equalizing waveforms for the sampled second signals and generating waveform-equalized third signals;

performing phase synchronization for the waveform-equalized third signals and generating phase-synchronized fourth signals;

generating a temporary target value that is an equalization target value of the phase-synchronized fourth signals and generating a fifth signal corresponding to the temporary target value;

generating a true target ~~value, that is~~ value from said fifth signal, the true target value being an equalization target value before performing phase synchronization~~, from said temporary target value~~ and generating a sixth signal corresponding to the true target value; and

computing tap factors for said waveform equalization from said sampled second signals, said waveform-equalized third signals and said sixth signal corresponding to the true target value.

13. (Currently Amended) The adaptive equalization circuit according to Claim 1, further comprising:

a frequency information threshold device for judging the frequency information of said phase synchronization device in a plurality of statuses using one or more threshold values;

a memory for storing tap factors corresponding to the statuses judged by said frequency information threshold device;

an equalization factor selection device for selecting either ~~the~~ an output of said first factor computation device or of said memory when a tap factor is supplied to said first digital equalization device;

a status time measurement device for measuring the duration of ~~said~~ a status ~~out~~ of the statuses judged by said frequency information and comparing ~~it~~ said duration with a predetermined value;

a factor computation control device for controlling the starting or stopping of the computation of said first factor computation device;

a factor memory storage processing device for transferring an instruction to stop the computation by said first factor computation device to said factor computation control device if said duration is longer than said predetermined value in said status time measurement device, and storing the tap factors after said factor computation device stops at a position corresponding to the status judged by said frequency information threshold device of said memory; and

a status change processing device for switching said equalization factor selection device so as to supply the tap factor to said first digital equalization device and notifying said factor computation control device that the computation by said first factor computation device is stopped if the tap factor corresponding to the status after change is stored in said memory when

the status judged by said frequency information threshold device changes, and for switching said equalization factor selection device so as to supply the tap factor~~, that is the computation result of said first factor computation device,~~ to said first digital equalization device and notifying said factor computation control device that the factor computation by said first factor computation device is started ~~if~~ when the tap factor corresponding to the status after change is not stored in said memory.

14. (Currently Amended) An adaptive equalization circuit, comprising:

an analog-digital conversion device for sampling signals read from a recording medium and for outputting first output signals;

a first digital equalization device for equalizing waveforms of the first output ~~of~~ signals from said analog-digital conversion device and outputting second output signals;

a phase synchronization device for synchronizing phases for said second output signals ~~equalized by~~ from said first digital equalization device and outputting third output signals;

a frequency information threshold device for judging frequency information of said phase synchronization device in a plurality of statuses using one or more threshold values;

a ~~second~~ memory for ~~previously~~ storing tap factors corresponding to the plurality of statuses judged by said frequency information threshold device respectively; and

a status change factor supply device for supplying a tap factor corresponding to said status to said first digital equalization device when the status judged by said frequency information threshold device changes.